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High-Speed Digital Control in a Switching-Synchronized Sampled-State Space for Variable Frequency Multi-Phase Buck Converters

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***Abstract*—This paper presents a new method for controlling variable frequency, multi-phase buck converters. At the MHz-range switching frequency for each phase, cycle-by-cycle digital control of current and voltage results in a fast transient response to and fast settling from disturbances. A key challenge in adding phases or increasing frequency is maintaining the ability to measure voltage without interference from switching transients; cycle-by-cycle voltage averaging is fast and largely impervious to these effects. Additional benefits include ease of design and implementation. Theory and modeling are presented and results are demonstrated in simulation.**

***Index Terms*—multi-phase, power converters, switching-sychronized sampled-state space, digital control, cycle-by-cycle averaging, voltage regulator modules.**

I. Introduction

A mounting demand for voltage regulator modules (VRMs) persists to enable the next generation of power distribution for high-performance GPUs and CPUs [1]. These VRMs need to be fast, while operating at increasingly lower voltages and higher currents. We can achieve these advanced capabilities by adding more converters and coordinating their phases. The demand for improved VRMs has spurred a resurgence in VRM-related research, including making digitally-controlled VRMs into ICs to implement at scale [2, 3]. Digital control is particularly attractive in this application because of programmability and, in turn, added flexibility.

Current research on multi-phase buck converters that operate at fixed-frequencies and utilize average current-mode control offer excellent current-sharing capabilities [4]. These designs leverage linear, together with fast nonlinear, controllers to offer exceptional speed in adapting to disturbances. However, these converters can have limited linear settling times due to their average current and voltage control schemes [4]. Other research presents mixed-signal (i.e., hybrid, analog and digital) peak current control with high-side current sensing, which is more challenging at high frequencies because of common-mode rejection [5]. Additionally, digital feedback control using output voltage point-sampling is susceptible to switching transients and interference. [3] demonstrates a multi-phase buck converter operating at variable frequency; this research exhibits an ultra-fast rise time but slower settling time because of a high-order loop transfer function from V_c to V_{out} and a sophisticated control scheme. Overall, constant on-time variable frequency converters that use valley-current control: (i) offer single-cycle current settling; (ii) avoid using slope compensation; and (iii) manifest quicker transient responses and settling [6].

In this paper, we present a multi-phase, variable frequency buck converter with digital control every phase-cycle. The switching-synchronized sampled-state space (5S) framework allows for a rigorous model, straightforward transfer functions, and compensation using direct digital design [6]. Invoking the valley-current for the current control loop enables ground-referenced current sensing, which ensures better common-mode rejection. The 5S-enabled phase-locked loop guarantees stability, quick-recovery after a transient, and automatic de-phasing that allows current to be delivered faster to the output.

The rest of this paper is organized as follows. Section II introduces the principles of operation and theory for 5S-enabled multi-phase buck converters. Section III includes simulations, and ongoing research involving a hardware demonstration is discussed in Section IV. The paper is concluded in Section V.

II. 5S Theory for Multi-Phase Buck Converters

The 5S framework enables high-speed, cycle-by-cycle voltage and current control of variable frequency converters [6]. In this paper, the 5S framework is applied to a multi-phase buck converter that has a constant switch on-time when the converter phase offsets are in equilibrium. Cycle-by-cycle average output voltage is measured using a high-speed analog differential hourglass integrator that does not need to reset, which will be discussed in further detail later in this section. With individual sensing of each inductor's valley current, we can achieve balanced currents among the converters in steady-state operation with phase-to-phase current commands for fast transient responses. The converter is shown in Fig. 1.

The controller design for a multi-phase buck converter involves both the phase control loop and the voltage control loop, both of which are discussed below.

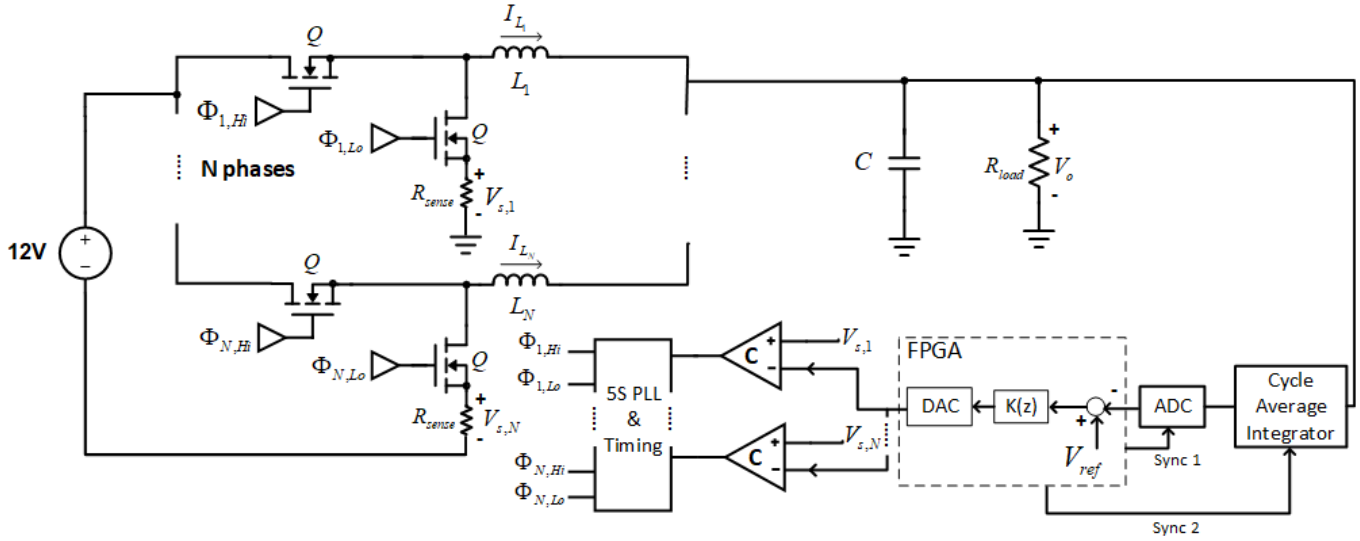

Figure 1: 5S Variable Frequency Constant On Time Multi-Phase Buck Converter

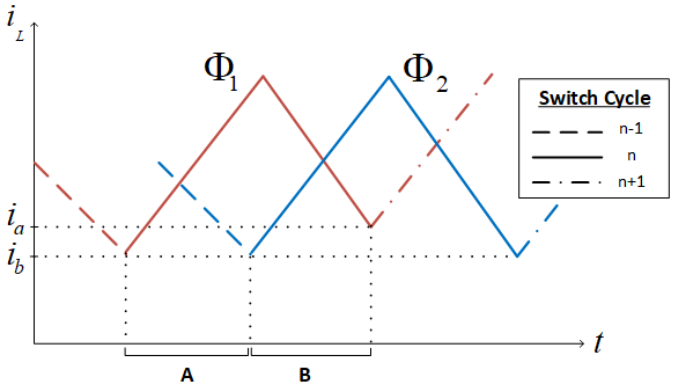

Figure 2: Synchronization of phases is achieved through the control of phase on-time for a setpoint time interval between valley currents of each phase.

A. Phase Control Loop

The 5S framework also can be applied to a high-speed phase-locked loop (PLL) to control the timing of each phase. The objective of the phase control loop is to interleave the phases of the inductor current waveforms. Given an N-phase buck converter, we make phase 1 have a constant on-time and be the reference for all the other phases (i.e., the *master* phase). Each of the subsequent follower phases (i.e., the *slave* phases) are locked to this reference with a phase offset (for $N = 4$, $\Delta\phi = 90°$) as illustrated in Fig. 2, where phase control is carried out by varying the on-time of these phases.

The switch cycles lose phase alignment during a transient when the off-times become necessarily different. The sum total of the integrated charge during interval A is used to determine the next valley current, which in this case is i_a. Similarly, the sum total of the charge integrated during interval B is used to determine the next valley current, which in this case is i_b. This same process of using the integrated charge during the time from one phase's valley to the next phase's valley is applied to N phases. Hence, the valley current instances determine the off-time.

The m^{th} follower phase is behind the master phase by a time delay $t_d^{(m,1)}$. The period of the m^{th} phase is denoted by $t_s^{(m)}$. The geometric relation illustrated in Fig. 3 yields

$$T_s^{(1)} + t_d^{(m,1)}[n] = t_s^{(m)}[n] + t_d^{(m,1)}[n-1]. \tag{1}$$

By denoting the on-time and duty cycle of the m^{th} phase $t_{\text{on}}^{(m)}$ and $D^{(m)}$, respectively, we have

$$t_{\text{on}}^{(m)}[n] = D^{(m)} t_s^{(m)}[n]. \tag{2}$$

Substituting (2) into (1) yields

$$t_d^{(m,1)}[n] = \frac{1}{D^{(m)}} t_{\text{on}}^{(m)}[n] + t_d^{(m,1)}[n-1] - T_s^{(1)}. \tag{3}$$

We denote the convergence point of the state trajectory $[t_d^{(m,1)}, t_s^{(m)}]$ by

$$T_d^{(m,1)} = \frac{m-1}{N} T_s^{(1)}, \tag{4}$$

$$T_s^{(m)} = \frac{1}{D^{(m)}} T_{\text{on}}^{(m)}. \tag{5}$$

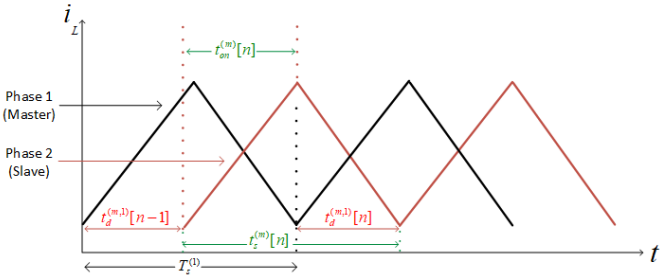

Figure 3: Phase control loop modeling for a multi-phase buck converter.

For ease of analysis, we can translate the origin of state trajectory to $[T_d^{(m,1)}, T_s^{(m)}]$. By defining

$$\tilde{t}_d^{(m,1)} = t_d^{(m,1)} - T_d^{(m,1)}, \quad \tilde{t}_s^{(m)} = t_s^{(m)} - T_s^{(m)}, \tag{6}$$

the current phase dynamics of the m^{th} phase is

$$\tilde{t}_d^{(m,1)}[n] = \tilde{t}_d^{(m,1)}[n-1] + \frac{1}{D^{(m)}}\tilde{t}_{\text{on}}^{(m)}[n], \tag{7}$$

$$\tilde{t}_s^{(m)}[n] = \frac{1}{D^{(m)}}\tilde{t}_{\text{on}}^{(m)}[n]. \tag{8}$$

We can then design the feedback control law as

$$\tilde{t}_{\text{on}}^{(m)}[n] = \alpha \tilde{t}_d^{(m,1)}[n-1]. \tag{9}$$

The closed-loop systems (7), (8) and (9) are asymptotically stable if

$$\left|1 + \frac{\alpha}{D^{(m)}}\right| < 1. \tag{10}$$

Furthermore, by selecting $\alpha = -D^{(m)}$, the phase dynamics are deadbeat. Therefore, the control law can be synthesized as

$$t_{\text{on}}^{(m)}[n] = -D^{(m)}\left(t_d^{(m,1)}[n] - \frac{m-1}{N}T_s^{(1)}\right) + D^{(m)}T_s^{(1)}. \tag{11}$$

For a multi-phase buck converter, all the phases share the same input and output voltages. We approximate the duty cycle $D^{(m)}$ by $D^{(1)}$, and the control law follows:

$$t_{\text{on}}^{(1)}[n] = -D^{(1)}\left(t_d^{(m,1)}[n] - \frac{m-1}{N}T_s^{(1)}\right) + D^{(1)}T_s^{(1)}. \tag{12}$$

B. Voltage Control Loop

The objective of the voltage control loop is to regulate the output voltage. We denote the time interval between the two adjacent valley currents by $t_m[n]$. The geometric relation illustrated in Fig. 4 yields

$$\sum_{i=0}^{N-1} t_m[n-i] = \frac{i_v[n-N] + m_1 T_{\text{on}} - i_v[n]}{m_2}. \tag{13}$$

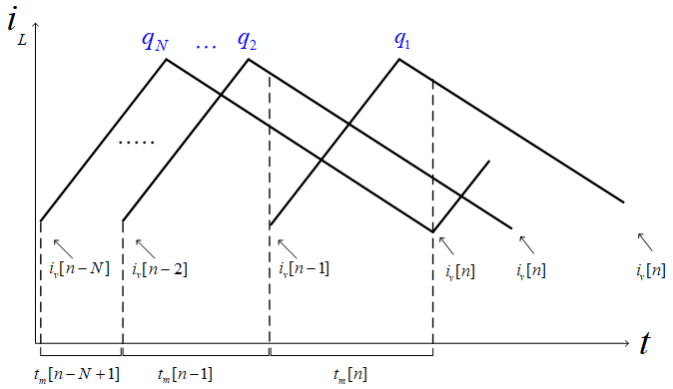

Figure 4: Small-signal model of the voltage control loop for a multi-phase buck converter.

Taking the z-transform of (13) yields

$$\frac{\tilde{t}_m(z)}{\tilde{i}_v(z)} = \frac{z^{-1}-1}{m_2}. \tag{14}$$

We denote the charge pumped to the output capacitor from the i^{th} phase during the time interval $t_m[n]$ by q_i. In the time interval $t_m[n]$, given the initial capacitor voltage $v[n]$, we can express the final capacitor voltage by

$$v[n+1] = v[n] + \frac{1}{C}\left(\sum_{i=1}^{N} q_i - \frac{v[n]}{R}t_m[n]\right). \tag{15}$$

When we obtain the equation for $v[n+1]$, $v[n]$, and $t_m[n]$, we notice that it reveals a nonlinear relationship between the valley current sequence and capacitor voltage sequence. To obtain a linearization about the operating point, we apply a small perturbation to this curve

$$\tilde{v}[n+1] = \left(1 - \frac{T_m}{RC}\right)\tilde{v}[n] + \frac{1}{C}\left(\sum_{i=1}^{n}\tilde{q}_i - \frac{V_{\text{out}}}{R}\tilde{t}_m[n]\right), \tag{16}$$

where T_m and V_{out} are the steady-state inductor-current valley-to-valley time interval $t_m[n]$ and capacitor voltage $v(t)$, respectively. Taking the z-transform of (16) yields

$$z\tilde{v}(z) = \left(1 - \frac{T_m}{RC}\right)\tilde{v}(z) + \frac{1}{C}\left(\sum_{i=1}^{n}\tilde{q}_i(z) - \frac{V_{\text{out}}}{R}\tilde{t}_m(z)\right). \tag{17}$$

We denote the inductor current trajectory in one switching cycle by $i_L(t; i_L(0), m_1, m_2, T_{\text{on}})$ [1]. i_L is a function of time and is parameterized by the initial current $i_L(0)$, inductor current rising ramp m_1, falling ramp m_2, and on-time T_{on}. Because m_1, m_2, and T_{on} are constant, we denote i_L by $i_L(t; i_L(0))$ for simplicity.

The charge that is pumped to the output capacitor by all phases can be calculated by

$$\sum_{i=1}^{N} q_i = \sum_{i=1}^{N} \int_{\sum_{j=1}^{i-1} t_m[n-j]}^{\sum_{j=0}^{i-1} t_m[n-j]} i_L(t; i_v[n-i])\, dt. \tag{18}$$

We now have the equation to relate q_i, t_m, and i_v. It reveals a non-linear relationship among the charge, time interval, and

[1] $i_L(t)$ starts at a current valley $i_L(0)$ where $t = 0$ and ends at the next current valley where $t = T_s$.

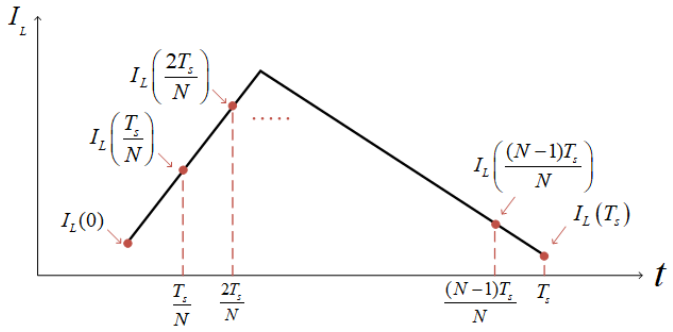

Figure 5: $I_L(t)$ represents the steady-state waveform of the inductor current trajectory in one switching cycle.

valley current. Again, we perform a small perturbation to this curve to obtain the linearization about the operating point

$$\begin{aligned}\sum_{i=1}^{N}\tilde{q}_i =& \sum_{i=1}^{N}\sum_{j=0}^{i-1}\tilde{t}_m[n-j]\; I_L(\frac{i}{N}T_s)\\ &-\sum_{i=1}^{N}\sum_{j=1}^{i-1}\tilde{t}_m[n-j]\; I_L(\frac{i-1}{N}T_s)\\ &+\frac{T_s}{N}\sum_{i=1}^{N}\tilde{i}_v[n-i],\end{aligned} \tag{19}$$

where T_s, V_{out}, and $I_L(t)$ represent the steady-state switching period $t_s[n]$, capacitor voltage $v(t)$, and inductor current trajectory $i_L(t)$, respectively. $I_L(t)$ is illustrated in Fig. 5.

Taking the z-transform of (19) yields

$$\begin{aligned}\sum_{i=1}^{N}\tilde{q}_i(z) =& \tilde{t}_m(z)\left(\sum_{k=0}^{N-1} I_L\left(\frac{k}{N}T_s\right)\right)\\ &-\tilde{t}_m(z)\left(\sum_{k=1}^{N-1} I_L\left(\frac{k}{N}T_s\right)\right)\sum_{k=0}^{N-1} z^{-k}\\ &+\frac{T_s}{N}\tilde{i}_v(z)\sum_{k=1}^{N} z^{-k}.\end{aligned} \tag{20}$$

Substituting (20) and (14) into (17) yields

$$\frac{\tilde{v}(z)}{\tilde{i}_v(z)} = \frac{\sum_{j=0}^{N} b_j z^{-j}}{1+a_1 z^{-1}} z^{-1}, \tag{21}$$

where

$$\begin{aligned} b_0 &= \frac{1}{C}\left(\frac{V_{\text{out}}}{R} - I_L(0)\right);\\ b_1 &= \frac{\sum_{k=1}^{N-1} I_L(\frac{k}{N}T_s)}{m_2 C} + \frac{I_L(0)-\frac{V_{\text{out}}}{R}}{m_2 C} + \frac{T_s}{NC};\\ b_j &= \frac{T_s}{NC} \qquad \forall\ 2 \le j \le N-1;\\ b_N &= -\frac{\sum_{k=1}^{N-1} I_L(\frac{k}{N}T_s)}{m_2 C};\\ a_1 &= -\left(1-\frac{T_s}{NRC}\right). \end{aligned} \tag{22}$$

C. Hourglass Integrator and Cycle-by-Cycle Averaging

To achieve phase-cycle averaging for the voltage control loop we use an hourglass integrator, which overcomes the traditional shortcomings that prevent the practical use of an integrate-and-dump circuit [7]. This cycle-averaging method is more robust to switching transients than point-voltage sampling, which requires careful positioning of time instance. The output voltage is integrated in the time intervals between the valley currents of every phase through the use of a down-counter in the FPGA. This allows for the fast inter-phase control derived in (21).

To begin, we start by defining the cycle-average voltage

$$\overline{v[n]} = \frac{v_s[n]}{t_m[n]}, \tag{23}$$

where $v_s[n]$ represents integration of the converter output voltage from the hourglass integrator, and $t_m[n]$ represents the integration time interval. This time interval is illustrated in Fig. 4.

$t_{\max}$ is the maximum integration time so that $t_m[n] \ll t_{\max}$. $t_m[n] \ll t_{\max}$ should also be selected so that

$$t_{\max} \gg T_{\max}/N, \tag{24}$$

where $T_{\max}$ is the maximum switching period for any converter phase.

$$t_{\max} = \frac{n_{\max}}{f_{\text{clk}}}, \tag{25}$$

where $n_{\max}$ is the maximum count for an FPGA counter implementation (e.g., $2^{16}-1 \approx 2^{16}$) and f_{clk} is the counter clock frequency.

In the digital domain, physical time is transformed to counter values n_s and $n_{\max}$ resulting in

$$\begin{aligned}\overline{v} &= v_s \times \frac{t_{\max}}{t_m} \times \frac{1}{t_{\max}}\\ &= v_s \times \frac{n_{\max}}{n_s} \times \frac{1}{t_{\max}},\end{aligned} \tag{26}$$

where $\overline{v} = \overline{v[n]}$, $t_m = t_m[n]$, $n_s = n_s[n]$, and $v_s = v_s[n]$.

A key challenge in implementing a cycle-average is digitally dividing the integrated voltage by the time interval, or equivalently the cycle interval. We can use approximations to avoid performing a computationally expensive division operation.

For (26), we can use an approximate hyperbola

$$\frac{1}{n_s} \approx \frac{n_{\max}-n_s}{n_{\max}}\, C_k. \tag{27}$$

By having $n_{\max}$ in the denominator and also a power of 2, the division is just a bit shift operation when implemented digitally. Furthermore, we want to ensure that the error is zero when the system is at equilibrium. We choose C_k to be a correction factor and n_s^* to be the equilibrium counter value

$$\frac{1}{n_s^*} = C_k \times \frac{n_{\max}-n_s^*}{n_{\max}} \tag{28}$$

$$C_k = \frac{n_{\max}}{n_s^*(n_{\max}-n_s^*)}. \tag{29}$$

In (28), the left-hand side represents the exact equilibrium value, and the right-hand side represents equilibrium value of the approximation with the correction factor. For $n_{\max} \gg n_s^*$,

$$C_k \approx \frac{1}{n_s^*}. \tag{30}$$

Therefore, we can combine (26), (29), and (30)

$$\overline{v} = v_s \times \underbrace{n_{\max} - n_s}_{\text{Down-Counter}} \times \underbrace{\frac{1}{t_{\max}} \times \frac{n_{\max}}{n_s^*}}_{\text{Pre-Calculated}} \times \underbrace{\frac{1}{n_{\max}}}_{\text{Bit-Shift}}. \tag{31}$$

Equation (31) can be implemented in an FPGA so that $n_{\max} - n_s$ is the output of a down-counter, requiring only two multiplications and a shift operation, which can typically be achieved in 3 FPGA clock cycles. It is worth noting that $n_{\max}$ is typically retained in the pre-calculation to maintain bit precision in the overall calculation.

A small-signal block diagram for the voltage control loop is shown in Fig. 6. The gain at equilibrium from the output of the hourglass integrator to the cycle-average voltage when using the approximation in (31) is

$$\begin{aligned} g_1^* &= \frac{\overline{v}}{v_s} = \frac{n_{\max} - n_s^*}{n_s^*} \frac{1}{t_{\max}} \\ &\approx \frac{n_{\max}}{n_s^*} \frac{1}{t_{\max}} \quad \text{for } n_{\max} \gg n_s^*. \end{aligned} \tag{32}$$

The variation of this gain from equilibrium n_s^* is

$$\begin{aligned} \delta g_1 &= \frac{n_{\max}}{n_s^*} \frac{1}{t_{\max}} - \left(\frac{n_{\max} - n_s}{n_s^*} \frac{1}{t_{\max}} \right) \\ &= \frac{n_s}{n_s^*} \frac{1}{t_{\max}}. \end{aligned} \tag{33}$$

From (32) and (33), the fractional gain variation

$$\frac{\delta g_1}{g_1^*} = \frac{n_s}{n_{\max}} \tag{34}$$

is small if one chooses $n_s \ll n_{\max}$. From a control robustness perspective, this means the variation in the loop gain from the cycle-average approximation will be small and additional gain margin is unnecessary in the compensation.

The circuit for the hardware implementation of the hourglass integrator is shown in Fig. 7; note that R_f is optional. For up-integration, analog switches 1 & 3 are ON and 2 & 4 are OFF; vice-versa for down-integration. Two hourglass integrators are interleaved so that while one is sampling the other holds its output and can be read by the ADC (analog-to-digital converter). The outputs of the hourglass integrators are multiplexed to a single ADC. The hourglass integrator waveforms are illustrated in Fig. 8. During the HOLD, i.e. flat portion, the input of the integrator is shorted so zero volts is integrated (e.g., switches 1, 2, 3, & 4 are all ON).

The hourglass integrator can continuously measure without resetting. If the output voltage of the integrator $v_{\text{ADC}}[n-1]$ is above zero, then the integrator down-integrates; for a voltage below zero, the integrator up-integrates. This allows the integrator differential voltage to continually center around zero.

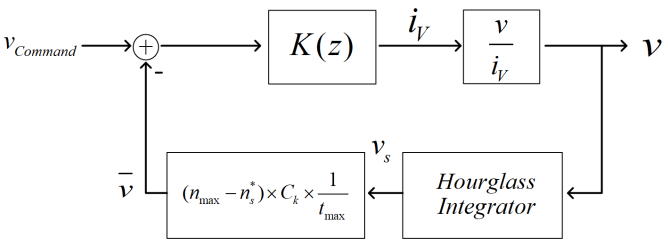

Figure 6: Small-signal block diagram for the voltage control loop including the hourglass integrator for cycle-by-cycle voltage control

The integrators in Fig. 8 perform an integration every $t_m[n]$ time period. $v_s[n]$ is the cycle integration that corresponds to the difference between the current ADC reading and the previous, i.e., $v_s[n] = v_{\text{ADC}}[n] - v_{\text{ADC}}[n-1]$. The integrator time constant $2RC_f$ must be chosen so that the integrator output does not saturate for the largest $v(t)$ and longest $t_m[n]$, where for the worst-case integrator, the output ramps from zero to $\pm v_{\text{Full-Scale}}$.

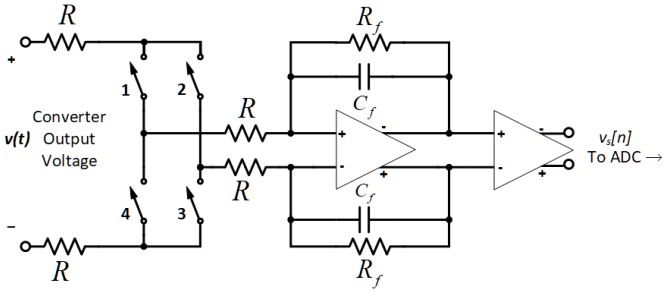

Figure 7: Hourglass integrator for phase-cycle-average voltage control.

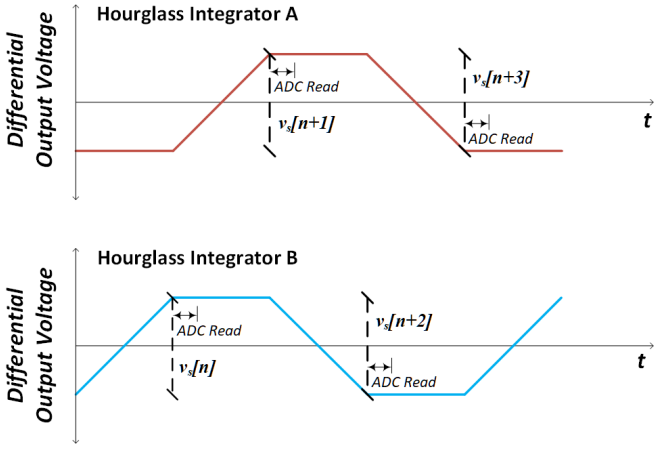

Figure 8: Interleaving of two hourglass integrator waveforms.

D. Compensation

For the 4-phase buck converter design in this paper, the plant transfer function for phase-cycle by phase-cycle control in (21) results in a pole-zero plot shown in Fig. 9; it is worth noting that three non-minimum phase zeros are evident. There

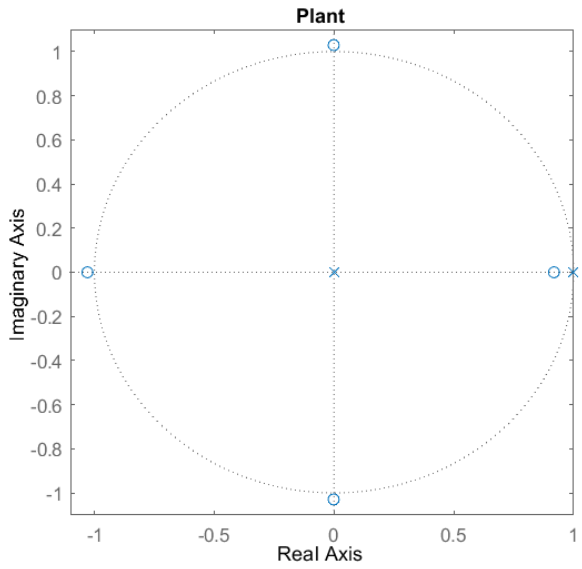

Figure 9: Converter plant pole-zero plot

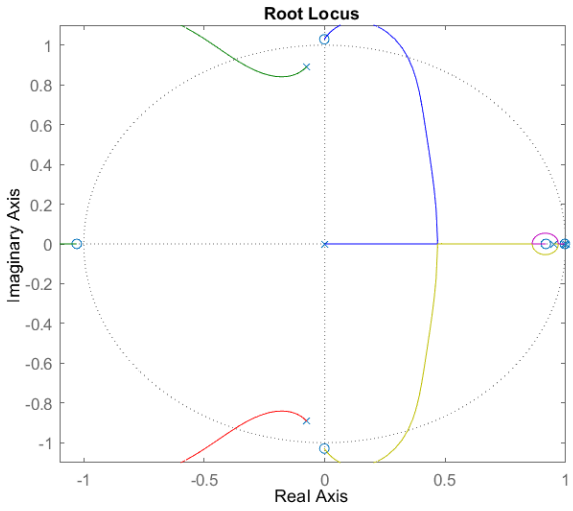

Figure 10: Root Locus for reference step compensation

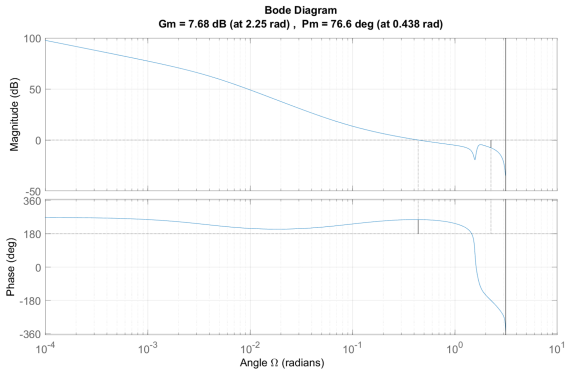

Figure 11: Bode Plot for reference step compensation

are four repeated poles at the origin each corresponding to a converter phase, a positive real zero, and the converter output RC filter's real pole.

To obtain the best transient response, i.e., fastest settling and smallest over/under-shoot, different compensation may be needed for reference step and load step performance. Good reference step performance is needed during dynamic voltage scaling (DVS), whereas good load step performance is needed during constant output voltage regulation. This form of scheduled-gain control is easily attainable with the programmability of digital controllers. Fig. 10 shows the root locus of the control loop transmission when compensated for good reference step response; the reference step response in the time domain is shown in Fig. 14. It is worth noting that the Bode plot illustrated for reference step compensation in Fig. 11 is plotted with respect to angle in the z-domain of 5S; it does not correspond to a physical frequency, but is a tool for designing the control loop.

Fig. 12 shows the root locus of the control loop transmission when compensated for good load step response; the load step response in the time domain is shown in Fig. 15. The 5S Bode plot for load step compensation is shown in Fig. 13

III. Simulation Case Study

A four-phase buck converter designed using 5S control was implemented in simulation with each phase operating at 1 MHz switching frequency. A reference step in Fig. 14 shows a risetime of 3 μs and a 1% settling of approximately 5 μs. The inductor currents de-phase as each independently provides the required current, which is updated after each phase's valley current, in response to the phase-by-phase cycle voltage error. The phases re-synchronize nearly as quickly as the voltage transient response. Additionally, a large-signal load step is simulated in Fig. 15, and shows an approximately 1.5 μs risetime, 1.25% undershoot and a 1% settling of approximately 8 μs. It is worth noting that because the converter phase significantly lose alignment, both the the reference step and load step are not small-signal.

IV. Ongoing Research

A 12 V to 1.8 V multi-phase buck converter is implemented with the parameters defined in Table I. A 15 MHz LTC2378 ADC is used with a single high-speed AD9744 DAC to set the valley current for all the phases. The digital controller is implemented in a Xilinx Artix 7 FPGA. Ultimately, 60 Watts will be delivered to the output. A photo of the experimental hardware setup is shown in Fig. 16.

V. Conclusion

We have presented a new method for controlling multi-phase, variable frequency buck converters within a 5S framework. Simulations show fast transient response and settling.

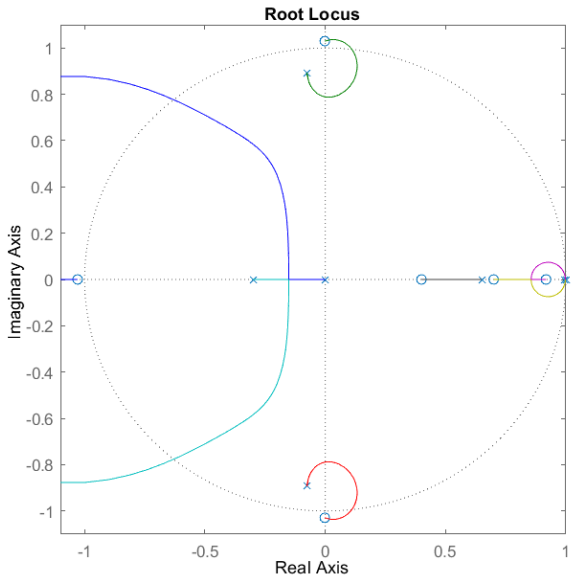

Figure 12: Root Locus for load step compensation

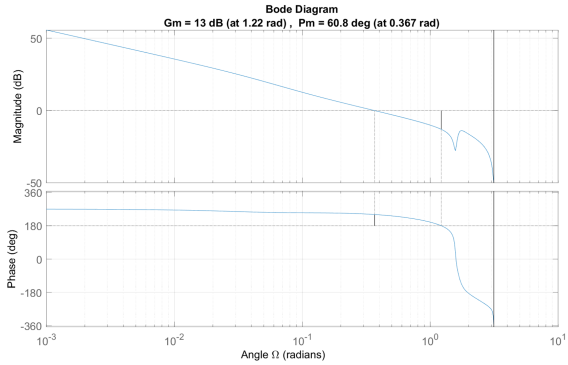

Figure 13: Bode Plot for load step compensation

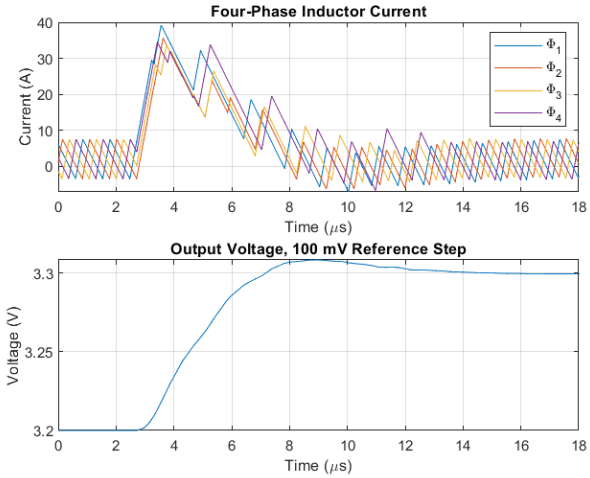

Figure 14: Simulation of phase timing and output voltage transient response for a 100 mV reference step.

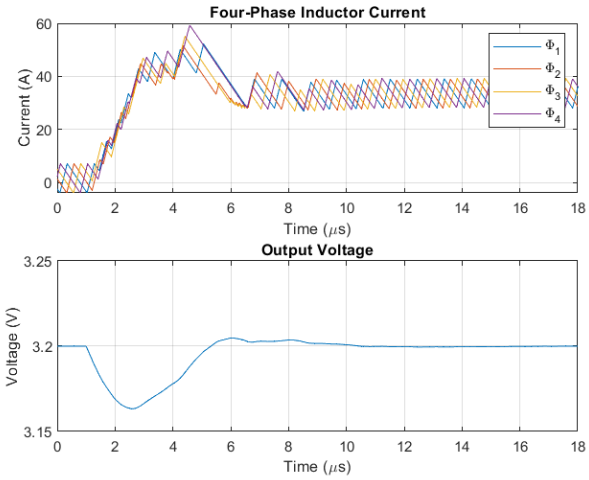

Figure 15: Simulation of phase timing and output voltage transient response and for a large-signal load step.

Table I: Hardware Prototype Parameters

Parameter	*Value/Type*
Input voltage	12 V
Output voltage	1.8 V
Inductor	200 nH
Output capacitance	813 uF
Load	50 mΩ
Switching frequency	1 MHz
On-time	150 ns

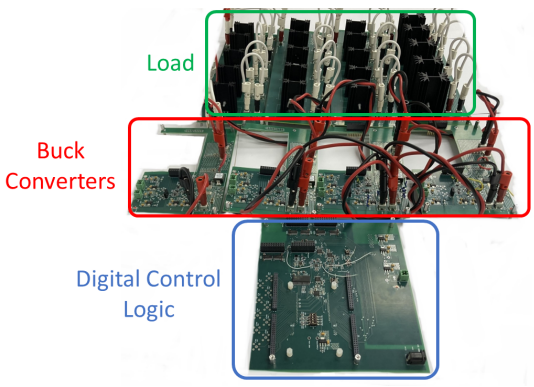

Figure 16: Multi-Phase Buck Converter Hardware Using 5S Digital Control.

REFERENCES

[1] E. R. Magsino, "Employing sliding mode control on a two-phase voltage regulator module," pp. 1–4, IEEE, 5 2021.

[2] T. Urkin and M. M. Peretz, "Digital multiphase pwm integrated module generated from a single synchronization source," pp. 1001–1007, IEEE, 6 2021.

[3] W.-C. Liu, C.-H. Cheng, C. Mi, and P. Mercier, "A novel ultrafast transient constant on-time buck converter for multiphase operation," *IEEE Transactions on Power Electronics*, vol. 36, pp. 13096–13106, 11 2021.

[4] B. Halivni and M. M. Peretz, "Digital controller for high-performance multiphase vrm with current balancing and

near-ideal transient response," pp. 2206–2213, IEEE, 3 2020.
[5] S. Kapat, "Sampling delay effect on stability in a multi-phase buck converter using digital current mode control," pp. 523–527, IEEE, 6 2021.
[6] X. Cui and A.-T. Avestruz, "A new framework for cycle-by-cycle digital control of megahertz-range variable frequency buck converters," pp. 1–8, IEEE, 6 2018.
[7] T. A. Denison, "The development of a nanoscale coulter counter for rapid genetic sequence recognition," 2000.